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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,386	12/01/2000	Naoto Horiguchi	001497	1274

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EXAMINER
TRAN, THIEN F

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,386	HORIGUCHI ET AL.	
	Examiner	Art Unit	
	Thien Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *4-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Objections

Claim 1 is objected to because of the following informalities: lines 9-10, "the tunneling phenomenon" should be --the direct tunneling phenomenon-- for lack of antecedent basis. Appropriate correction is required.

Claim 3 is objected to because of the following informalities: line 4, "the tunneling phenomenon" should be --the direct tunneling phenomenon-- for lack of antecedent basis. Appropriate correction is required.

Claim 12 is objected to because of the following informalities: lines 8-9, "the tunneling phenomenon" should be --a direct tunneling phenomenon-- for lack of antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Park (USPN 5,770,877).

Park discloses a semiconductor memory (Fig. 11i) comprising a semiconductor substrate 10; a tunneling insulating film 16 formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a tunneling phenomenon (Fowler-Nordheim tunneling); a floating gate electrode 13 formed on said tunneling insulating film; a gate insulating film (16, 17) covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, wherein said gate insulating film has a thickness which is thicker than the tunneling insulating film 16 so it is inherent that carriers are not allowed to transmit therethrough by the tunneling phenomenon; a first control gate electrode 12 disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and a pair of impurity doped regions 14 formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode, wherein a surface layer of said semiconductor substrate under said first control gate electrode 12 has a conductivity (p type 10) opposite to that of said impurity dope regions (n type 14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (USPN 5,770,877) in view of Hu et al. (USPN 5,511,020 of record).

Park as described above does not disclose the tunneling insulating film 16 having a thickness thin enough to transmit carriers therethrough by a direct tunneling phenomenon. Hu et al. discloses a nonvolatile memory device (Fig. 1) having a thin direct tunneling dielectric 102 with a thickness between 1.5 nm and 5 nm. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the memory device of Park having a thin direct tunneling insulating film as taught by Hu et al., wherein the thin dielectric tunneling insulating film has a thickness between 1.5 to 5 nm in order to provide a memory device having a high density, increased write/erase speed, and increased endurance. As a result, the thin direct tunneling insulating film allows carriers therethrough by a direct tunneling phenomenon.

Regarding claim 3, Park further discloses a dielectric film 17 formed on an upper surface of said floating gate electrode, said dielectric film having a conventional thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon; and a second control gate electrode (a portion of the word line 12 on the floating gate electrode 13) formed on said dielectric film and electrically connected to said first control gate electrode (a portion of the word line 12 over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode), said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park (USPN 5,770,877) in view of Hu et al. (USPN 5,511,020 of record) as applied to claim 1 above, and further in view of Shigyo (USPN 6,222,224 of record).

Park in view of Hu et al. as described above do not explicitly disclose materials of said floating gate electrode and a channel region between said pair of impurity doped regions being selected so that a Fermi level of said floating gate electrode is in a forbidden band (band gap) of the channel region when an external voltage is not applied between the channel region and said first control gate electrode. Shigyo discloses a semiconductor memory (Figs. 1A-1C) comprising a channel region 27 and a floating gate electrode 11 made of materials that provide a Fermi level at substantially the center of the band gap of the channel region (see Fig. 7 and col. 8, lines 39-50). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the floating gate electrode and the channel region of materials as taught by Shigyo in order to provide a Fermi level at substantially the center of the band gap of the channel region and increase the reliability of the memory. Since the modified Park provides the claimed structure having the materials that provide the Fermi level of the floating gate electrode in a forbidden band as claimed, it is inherent that a Fermi level of the floating gate electrode is obtained in a forbidden band of the channel region when an external voltage is not applied between the channel region and the first control gate electrode.

Response to Arguments

Applicant's arguments, see Paper No. 11, filed 03/31/2003, with respect to the rejection(s)of claim(s) 1-3 and 12-14 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Park, Hu et al. and Shigyo references.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt
April 23, 2003

Thien Tran
Patent Examiner
Technology Center 2800